REMARKS

In the Official Action mailed 15 December 2005, the Examiner reviewed claims 1-4. The Examiner has rejected claim3 under 35 U.S.C. §112, second paragraph; and has rejected claims 1-4 under 35 U.S.C. §103(a).

Each objection and rejection is respectfully traversed below.

Report of Telephonic Interview

On March 14, 2006, a telephonic interview was held to discuss the Yang et al. reference, on which the Examiner relied as a primary reference. Applicants directed the Examiner's attention to column 3, about line 45, which describes the several pillars 15 as being randomly located within the cavity. Because sputtering of polymer byproducts on a surface (col. 3, lines 29-32) is a matter of chemistry and acknowledged to be "random", the enabling characteristics of the Yang reference are better considered under the chemical arts principles than as normally done in semi-conductor manufacturing cases. No empirical results are reported by Yang to predict the number of pillars randomly created or the process variability introduced.

Applicants characterized Yang as taking a process defect and labeling it a feature. Other than to create a random number generator, who in their right mind would select a process designed to produce random capacitance? Given that capacitance is related to conductor surface area, introducing random numbers and placements of "pillars" in would necessarily lead to random capacitance.

The Examiner suggested that Applicants supply some objective commentary on the desirability of process uniformity and consistence. Applicants indicated that they could do so.

No agreements were reached. Applicants invited the Examiner to call with any suggested amendments, when the case next comes up on his docket.

Rejection of Claim 3 under 35 U.S.C. §112, second paragraph

The Examiner has rejected claim 3 under 35 U.S.C. §112, second paragraph, because claim 3 recites the limitation "the first conductive layer" in line 10. The wording has been amended to correct a typographical error and substitute "metal plate" for "conductive". Accordingly, reconsideration of the rejection of claim 3 as amended is respectfully requested.

Rejection of Claims 1-4 under 35 U.S.C. §103(a)

The Examiner has rejected claims 1-4 under 35 U.S.C. §103(a) as being unpatentable over Yang et al. (US Patent No. 5,804,489) in view of Agarwal et al. (US Patent No. 6,297,527).

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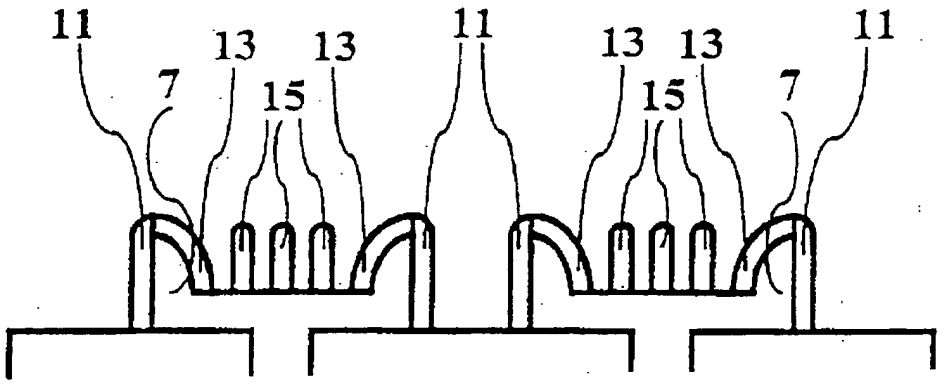
Claim 1 includes the limitations, "a wave-shaped pattern in the base conductive layer comprising at least two adjacent trenches in the base conductive layer". The spaces between "random" pillars in Yang (col. 3:44-46) would not be considered by one of skill in the art to be trenches. In the art, trenches are features that are deliberately patterned in a surface. The term "trenches" is not used in the art to refer to random structures caused by uncontrolled sputtering of polymers that interferes with etching.

The combination of Yang and Agarwal does not render the claimed invention obvious. Random capacitance generated by "random" pillars in Yang overlaid by Agarwal's carefully engineered features does not render the claimed structure obvious, because the resulting combination does not produce the desirable capacitance features that one of skill in the art would recognized from the words of the claim. Random capacitance from combining Yang in view of Agarwal would not be interchangeable with or render obvious the claimed structure.

The proposed combination does not have a reasonable likelihood of working, due to the random spacing (col. 3:44-46) of Yang's pillars. The random spacing does not support deposition of Agarwal's multiple layer structure. The illustration in Yang FIG. 5 gives the sense of closely spaced pillars, albeit illustrated in a misleading way, because the pillars are depicted as uniformly spaced, even though the text explains that their creation and spacing are random:



Yang illustrates sidewall residue **13** illustrated as having the same thickness as the space between pillars **15**. Residues found in position **13** tend in semiconductor processing to be thin. Yang does not illustrate any deposition layers that are thinner or narrower than **13**, **15** or the random spacing between pillars **15**. At most, Yang allows one deposition layer to fill the space between random pillars **15**. Yang expressly teaches covering all of the pillars in one layer, in FIG. 7.

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There is no basis for assuming that Agarwal's six-layer (by two) build-up could reliably be built between Yang's pillars **15**. One of skill in the art would not expect twelve layers (depicted in Agarwal FIG. 21) to fit between randomly spaced pillars **15**. The proposed combination does not have a reasonable likelihood of success, based on the information that Yang provides.

The combination is improper, because one of skill in the art would not be motivated to use Yang as a base reference for producing 64-Mbit DRAM cells as described in Agarwal (col. 1, lines 35-38). Variability in the number of columns and amount of capacitance of individual capacitors would not encourage formation of a complex structure over the random pillars.

Substantial literature regarding process reliability and the desirability of "precise capacitors" and capacitors having "matched capacitance" teaches away from the combination. The attached excerpts from Van Zant, Microchip Fabrication Third Edition (McGraw-Hill 1997) emphasize critical dimension budgets and error budgets (at 281), "exact dimension required of each component in the circuit" (at 446). "For products with submicron minimum feature sizes, the CD tolerances are 10 to 15 percent" (at 281), which is too tight a budget to allow for random pillars. An example of a reference discussing the need for "precise capacitors" include Dunn US 6,606,793 B1, col. 1:35, and a word search of patent databases produces many more references. Example of references that refer to matched capacitors include Zhang et al., US 6,366,230 B1, col. 6:23-46 and Sakurai et al., US 6,614,645 B1, abstract and *passim*. This is evidence that one of skill in the art will not select Yang's random pillars as the basis for building usable capacitors. One of skill in the art would not combine Yang with Agarwal (or any other reference) to produce the claimed structure.

Further regarding claim 3, Agarwal teaches away from the claimed use of the base conductive layer as the first conductive layer, preferring a specific multilayer first conductive layer.

Accordingly, reconsideration of the rejection of claims 1-4 is respectfully requested.

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CONCLUSION

The Examiner has conducted two searches and not really found a good primary reference. Assuming that some sort of supplemental search will be conducted, after a first RCE already has been filed, Applicants request that the Examiner call the undersigned to discuss any additional references that might be cited and any amendments that might be suggested.

It is respectfully submitted that, in the absence of additional references, this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1518-2).

Respectfully submitted,

Dated: 15 March 2006

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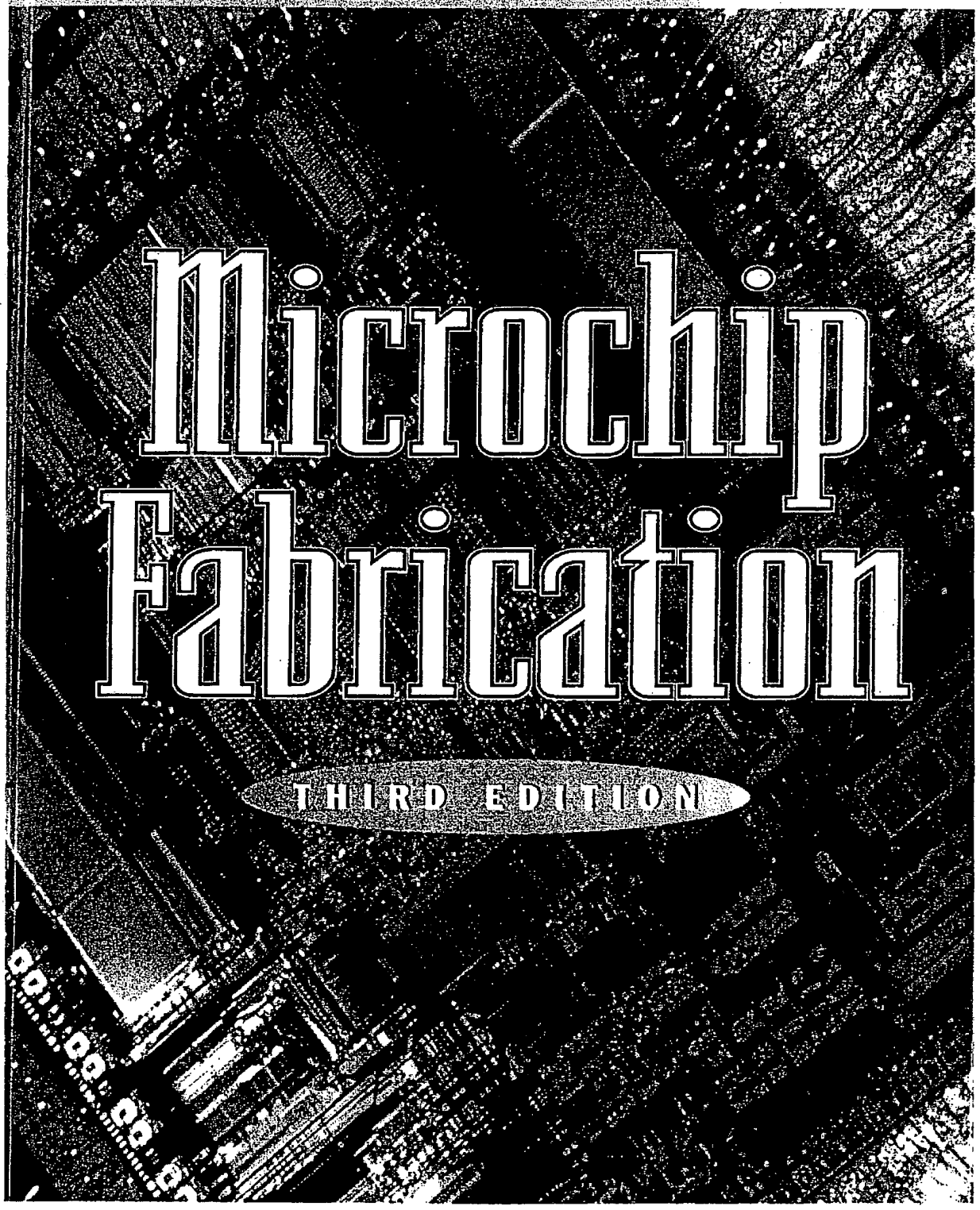
Attorney Docket No. MXIC 1518-2

APPLICATION NO. 10/695,167

ATTACHMENT TO AMENDMENT DATED 15 MARCH 2006

PETER VAN ZANT



A PRACTICAL GUIDE TO
SEMICONDUCTOR PROCESSING

Microchip Fabrication

A Practical Guide to Semiconductor Processing

Peter Van Zant

Third Edition

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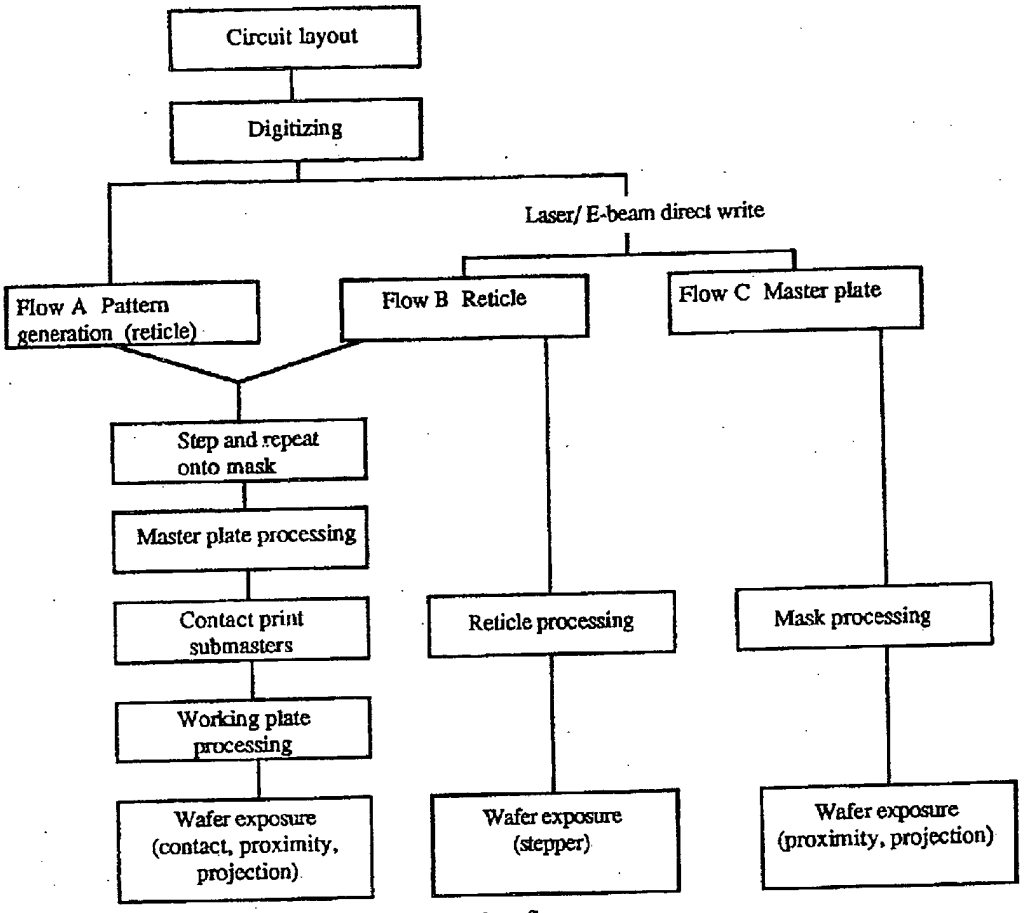

Figure 9.31 Mask/reticle-making processing flows.

cases, the reticle or mask is processed to etch the pattern into the chrome.

Other mask and reticle process flows may be employed. The reticle in Flow A or the master plate may be laser or e-beam generated.

VLSI- and ULSI-level circuits require virtually defect-free and dimensionally perfect masks and reticles. Critical dimension (CD) budgets from all sources are 10 percent or better leaving the reticles with a 4 percent error margin.[34] There are procedures to eliminate unwanted chrome spots and pattern protrusions with laser "zapping" techniques. There is also a technology to fill in missing pattern parts and fill pinholes by using focused ion beams (FIB).

Summary

For VLSI and ULSI work, the resolution and registration requirements are very stringent. In 1977, the minimum feature size was

3 μm. By the mid-1980s, it had passed the 1-μm barrier. By the 1990s, 0.5-μm sizes were common with 0.35-μm technology planned for production circuits. Circuit design projections call for minimum feature sizes less than 0.1 μm.[35]

Chip manufacturers calculate several budgets for each circuit product. A *critical dimension* (CD) *budget* calculates the allowable variation in the image dimensions on the wafer surface. For products with submicron minimum feature sizes, the CD tolerances are 10 to 15 percent.[36] Also of concern is the critical defect size relative to the minimum feature size. These two parameters are brought together in an *error budget* calculated for the product. An *overlay budget* is the allowable accumulated alignment error for the entire mask set. A rule of thumb is that circuits with micron or submicron feature sizes must meet registration tolerances of one-third the minimum feature. For a 0.35-μm product, the allowable overlay budget is about 0.1 μm.[37]

Key Concepts and Terms

Develop inspect and rework
Dry etch methods
Dry stripping
Error budget
Etch process
Final inspect
Hard bake methods
Hard bake process
Immersion develop
Mask making
Negative resist developers
Overlay budget
Plasma descum
Positive resist developers
Puddle develop
Resist development
Resist stripping
Spray develop
Wet etch methods
Wet strip chemicals

Review Questions

1. Name the major methods of resist development.
2. What are the chemicals used to develop negative and positive resists?
3. What is the purpose of the hard bake step?
4. Name three methods used for hard bake.
5. What problems arise if the hard bake temperature is too low? Too high?
6. Name the preferred wet etchants for etching silicon dioxide layers, silicon nitride layers, and aluminum layers.

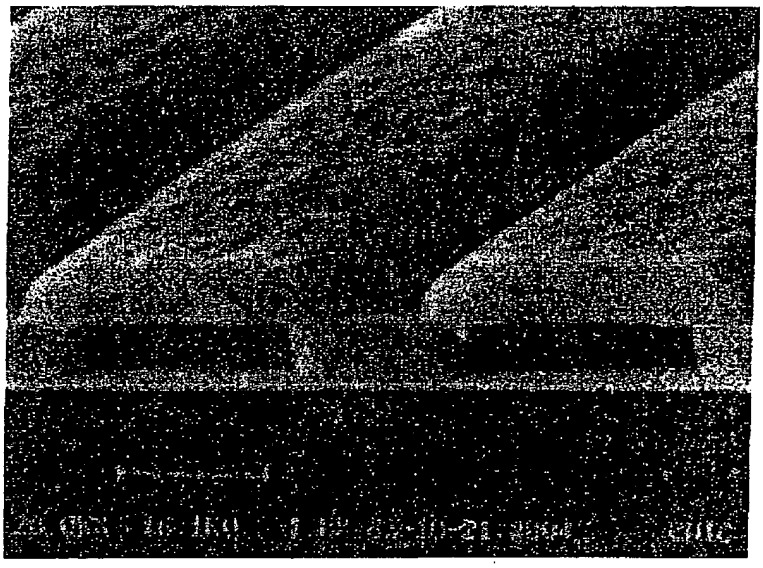

Figure 14.29 SEM declination of device cross section.

down through the junction, junction depth can be determined by monitoring the dopant atoms as they disappear from the stream.

Scanning capacitance microscope (SCM)

One of the options with the atomic force microscope (AFM), see "General Surface Characterization") is a probe that measures capacitance. Since the capacitance of a doped layer changes as the junction is approached, the probe can be used for junction depth detection. Sample preparation is the same as that for spreading resistance measurements.

SCM offers the advantage of nanometer precision[8] and, in the near future, may be the concentration profile and junction depth measurement technique for submicron junctions.

ritical Dimensions (CD) and Line Width easurements

he exact dimensions required of each component in the circuit are ontrolled and influenced by *all* processes. Vertical dimensions are set y the doping and layering processes. The horizontal surface dimenions are produced in the photomasking area. As part of that process, ne critical dimensions are measured at both develop inspection and nal inspection with microscopes.

Filar mechanical measuring eyepiece

The filar measuring eyepiece is a dimension-measuring instrument that is fitted to a microscope. The eyepiece features a movable hairline that requires calibration to an outside standard. A calculation is made to "correct" the filar measurements to the actual dimensions on the standard.

The pattern to be measured is focused in the field of view (Fig. 14.30). A hairline is positioned perpendicular to the measuring location path. Once oriented, the hairline is moved to the starting point of the pattern to be measured, and the value on the micrometer barrel is noted. The hairline is then moved in a smooth continuous motion to the other side of the pattern. The ending value is also noted. The actual width is calculated by subtracting the starting value from the ending value and multiplying the resulting number by the previously determined correction factor. This system is highly accurate and is used by the National Bureau of Standards. Accurate measurements require good operator techniques.

Filar systems are easily automated. The hairline movement mechanism can be motorized and the correction factor programmed into an onboard computer, resulting in a direct digital readout of the actual width. Operator fatigue is minimized by a video monitor rather than requiring the operator to view the wafer through a high-power microscope.

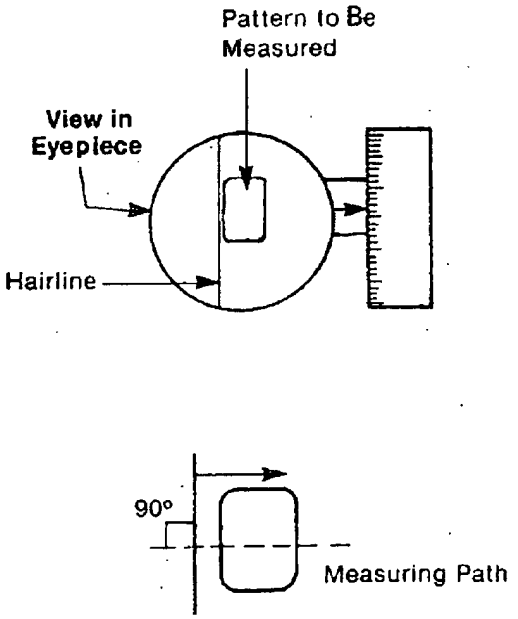

Figure 14.30 Manual filar width measurement.

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